IN THE DRAWINGS:

Please enter substitute drawing sheet 1 of 2 provided herewith, comprising Figures 1 and 2 that have been modified as indicated to correct informalities with respect to element numbers 28 and 30. These drawings are labeled as "Annotated" sheets as per the Examiner's indication.

REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Office Action of May 2, 2005, which action constitutes a Final Rejection, the Examiner first objected to Claim 6 as amended in applicants prior response submitted December 28, 2004 as not properly indicated with the label "Currently Amended". In response, Applicants respectfully resubmit the amendment to Claim 6 with the proper indication as "Currently Amended". The Examiner is respectfully requested to remove the objection to Claim 6. Further in the Office Action, the Examiner objected to Claim 16 as essentially not conforming to applicants' amendment to method steps in independent Claim 11 as submitted in applicants prior response of December 28, 2004. Applicants respectfully take this opportunity to correct this informality and request that the Examiner remove this objection to Claim 16.

Further in the Office Action, the Examiner alleged that the amendment to drawing sheet 1 including Figures 1 and 2 that was submitted in applicants prior response of December 28, 2004 was improper as the amendment constituted submission of an "Annotated" drawing sheet and the amended drawing sheet was not so labeled. Applicants respectfully request entry of the same drawing amendment, this time, with the designation as an "Annotated" drawing sheet. It is respectfully requested that the Examiner remove this drawing objection.

Further in the Final Rejection of May 2, 2005, the Examiner further rejected independent Claims 1 and 11 under 35 U.S.C. §102(b), as being allegedly anticipated by Tamura et al. (US 6,247,138 B1)(hereinafter "Tamura").

The Examiner further rejected dependent Claims 2, 12 and 18 under 35 U.S.C. §103(a), as being allegedly being unpatentable over Tamura as applied to Claim 1 in further view

of Rogers (US 5,982,210) (hereinafter "Rogers"). Claim 3 was further rejected under 35 U.S.C. §103(a) as being allegedly being unpatentable over Tamura in view of Li et al. (US 5,477,181) (hereinafter "Li"). Claims 4 and 13 were additionally rejected under 35 U.S.C. §103(a) as being allegedly being unpatentable over Tamura and Rogers in further view of Ornes et al. (US 6,748,567) (hereinafter "Ornes"). Claims 5 and 14 were additionally rejected under 35 U.S.C. §103(a) as being allegedly being unpatentable over Tamura and Rogers in further view of Mergenthaler et al. (US 4,070,648) (hereinafter "Mergenthaler"). The Examiner further rejected the remaining claims largely based on combinations with Tamura, Rogers and other references.

Applicants respectfully request entry of this amendment after FINAL REJECTION, largely to clarify the subject matter of the invention as embodied in the claims of the present application and to address the Examiner's reference to Tamura and Rogers which have only been cited and applied for the first time in this FINAL REJECTION. As the Examiner for the first time has applied these references in this FINAL REJECTION, entry of this response to address the merits of the newly cited references is respectfully requested.

With respect to the rejection of Claims 1 and 11, applicants respectfully disagree. As a preliminary matter, Claims 1 and 11 are being amended to clarify that the clock signal is provided to the IC's transmitter means and the receiver device, in the manner that the clock timing signal times data signal transmission and reception within said IC at successively different clock speeds and, that the adjusting means adjusts the clock timing signal provided to the respective transmitter means and said receiver device at each clock speed, wherein the clock timing signal is adjusted to achieve a maximum speed allowed for the IC that avoids a data transmission fail point during real-time operation. This is clearly shown in each of the drawing Figures 1 and 2 and respectfully no new matter is being added by this amendment.

Respectively Tamura does not teach or suggest such a system.

In Tamura, as shown in Figure 2, for instance, a single reference lock signal CLK*i* is provided to the transmitter logic circuit 24 and receiver logic circuit 25 used in generating signals for data transmission and receipt. This reference clock signal CLK*i* provided to the transmitter logic circuit 24 and receiver logic circuit 25 is constant and not changed at all the during operation and is not used to determine optimum clock speeds for maximizing speed of successful data transmissions within the IC. In Tamura, rather, a separate timing generator circuit is provided to receive the reference clock signal and alter the timing of a control signal generated by the transmitting logic circuit 24 that is to be received by a separate circuit, i.e., a DRAM core 3 as shown in Figure 2 of Tamura. Thus, in Tamura, based on the signal reference clock, a means is provided (counters and delays) to generate two or more additional clocks (i.e., phase differentiated to have respective different rising and falling edges, for example) that are utilized to adjust a set activation period for controlling DRAM operation. That is, in Tamura, a plurality of additional clocks are generated (in block 26 of Figure 2) of which two different clock signals may be used to adjust an activation/deactivation command of the control signal CNT (see Tamura, col. 2, lines 11-24). This "altered" timing control signal provided to the DRAM, i.e., signal CNT, is not a clock signal nor is it used to alter transmission and reception speeds of devices within the IC in order to optimize (i.e., maximize) speed of the transmitter/receiver data communications.

Thus, Tamura can not be anticipatory, for the following reasons:

1) Tamara does not teach the limitations of Claim 1 (and Claim 11) directed to providing a clock signal to an IC's transmitter means and the receiver device, in the manner such that the clock timing signal times data signal transmission and reception within said IC at

successively different clock speeds with each successive data signal transmission transmitted at a different clock speed;

2) Tamara does not teach the limitations of Claim 1 (and Claim 11) directed to providing a monitoring circuit means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and,

3) Tamara does not teach the limitations of Claim 1 (and Claim 11) directed to (means for) adjusting said clock timing signal provided to both the transmitter means and said receiver device at each clock speed, the clock timing signal adjusted to achieve a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation. At best, according to Tamura's second embodiment teaching of Figures 11-13 (cols. 17 19 of Tamura), data transmission/reception timing on a single data line may be altered to address data line skew phenomena only by providing a plurality of timing adjusting circuits (Figs. 11) in one-to-one correspondence with each data line, e.g., either on the transmitting side or receiving side, to generate a plurality of respective clock signals of which one clock may adjusted to correct the skew on that associated single data line. Respectfully, this is not suggestive of coordinating a signal clock signal out of a plurality of successively generated signals that is input to both transmitter and receiver wherein the clock signal is of a speed that is optimized for data transmission after detecting a signal transmission fail point at a particular clock speed.

As Tamura does not teach each of these claim limitations, the Examiner is respectfully requested to withdraw the rejection of Claims 1 and, likewise, Claim 11 under 35 U.S.C. §102(b).

Due to the novel aspects of Claims 1 and 11 herein amended for clarification purposes and setting forth limitations that are neither taught nor suggested by Tamura, Applicants respectfully to

withdraw corresponding rejections of dependent Claims 2-10 and 12-18. With specific reference to the applied Rogers and Ornes references, e.g., in the rejection of Claims 4 and 13, applicants respectfully disagree and submit the Examiner's reliance on these references is misplaced. For instance, Rogers provides an improved PLL clock generator for seamlessly changing a frequency of an output clock signal between high and low transitions, i.e., between active (fast) mode to a slow mode, and only in a manner that ensures synchronicity- i.e., that the clock signals are synchronous. While feedback is provided to phase lock loop in the form of a "peripheral" clock signal, there is no teaching or suggestion that this signal is used to adjust a clock input to both an IC's transmitter means and the receiver device at different clock speeds, nor does it represent a signal used to adjust a clock timing signal to achieve a maximum operating speed after detection of a clock operating speed that causes a data transmission failure point. Moreover, the use of ECC circuitry as taught in Ornes and relied upon by the Examiner in the rejection of Claims 4 and 13 is misplaced. Ornes relates to "packet" communications in an optical fiber, wired or wireless communications system that rely upon clock recovery, i.e., and is not used for the purposes of detecting a data transmission fail point when ECC codes are generated and detected at operating speeds adjusted according at successively different transmitter and receiver clock speeds, much less used for maximizing the timing between a transmitter and receiver on the same IC. That is, Ornes in combination with Rogers and Tamura is not suggestive of the claimed combinations of Claims 1,2 and 4 and Claims 11, 12 and 13 as the applied combination of references does not teach provision of feedback for adjusting clock speeds at both transmitter and receiver devices to achieve a maximum speed allowed for the IC that avoids a data transmission fail point based on ECC signal transmission/detection of an ECC error as claimed in the present invention.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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SF:gc:cm

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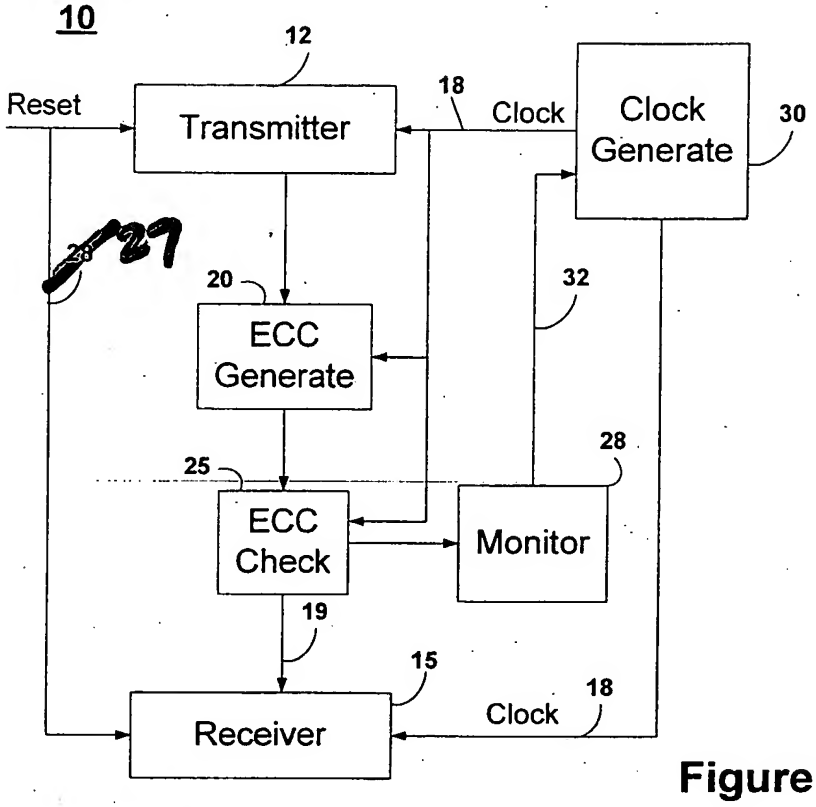

Figure 1

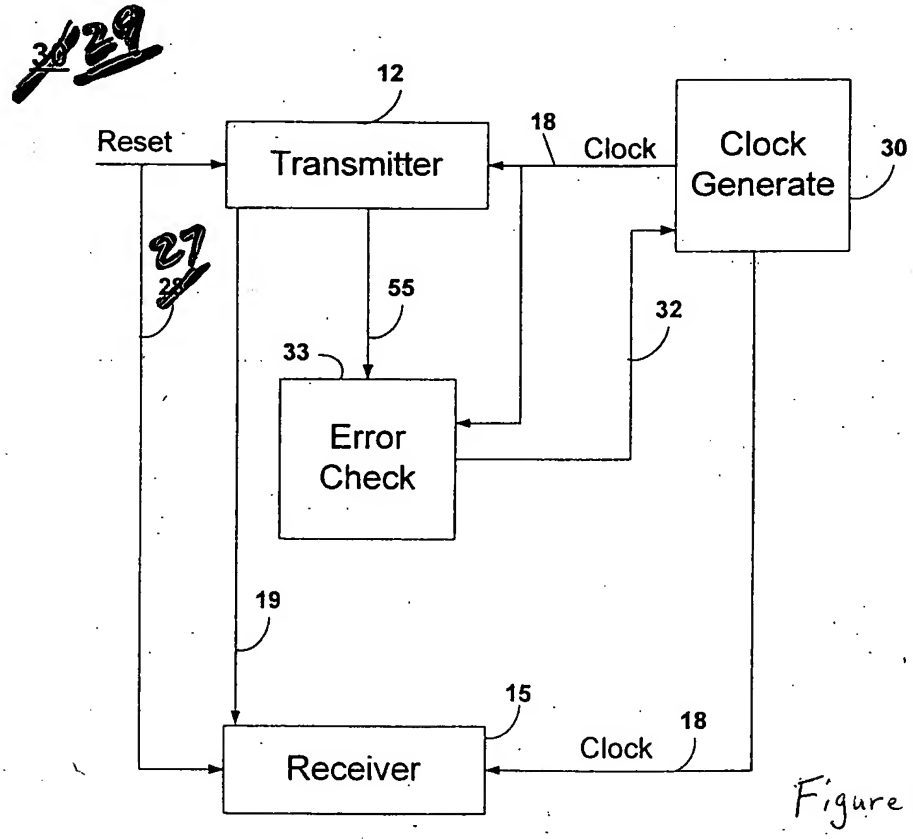

Figure 2